UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/859,575	05/15/2001	William J. Hamilton JR.	PD-00W071	4120

7590 06/05/2002

Raytheon Company
Intellectual Property
MC Eo/El/E150
P.O. Box 902
El Segundo, CA 90245

EXAMINER	
YAM, STEPHEN K	
ART UNIT	PAPER NUMBER
2878	

DATE MAILED: 06/05/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/859,575	HAMILTON ET AL.	
	Examiner	Art Unit	
	Stephen Yam	2878	

-- The MAILING DATE f this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-23 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-23 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 14 September 2001 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Objections

1. In Claim 15, the phrase "is selected" on line 2 is repeated. One instance of the phrase should be deleted.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claim 20 lacks antecedent basis in the limitation "the semiconductor region" in lines 3-4.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3, 4, and 6 are rejected under 35 U.S.C. 102(b) as being unpatentable by Cigna et al. US Patent No. 5,591,959.

Regarding Claim 1, Cigna et al. teach a detection array structure with an array of supported islands (see Fig. 2D, ref. 16 and 18) comprising a first region (left-instance of 22) physically discontinuous from the first region of each of the other supported islands and a second region (right-instance of 22) physically discontinuous from the second region of each of the other

supported islands. Cigna et al. also teach a bump interconnect structure comprising a first and second bump interconnect extending from the first and second regions respectively, attaching through a first and second interconnect location respectively, to an element (20) of a interconnect array (58) (see Fig. 3). Although Cigna et al. does not specifically mention that the interconnect array is constructed of a microelectronic integrated circuit, it is inherent that an interconnect array is constructed using microelectronic integrated circuit means.

Regarding Claim 3, it is inherent that an interconnect array provides an electrical interface between the detectors and any external elements since the interconnect array serves as a readout device and is constructed of microelectronics. In addition, Cigna et al. teach the first and second regions as input/output elements (see Col. 3, lines 48-51).

Regarding Claim 4, Cigna et al. teach the hybridization of the detector elements (see Col. 4, lines 6-8). Therefore, it is inherent that an interconnect array in a detector array is used as a readout device in a hybrid detector array. Cigna et al. also teach the input/output element as a detector (see Col. 3, lines 48-51).

Regarding Claim 6, Fig. 3 shows the array structure (58) to be planar.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 2, 5, 8-9, 12, and 16-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cigna et al.

Regarding Claims 2, 8, and 12, Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect used to hybridize the islands (see Col. 4, lines 6-8). Cigna et al. also teach the interconnect array and detector array being substantially planar, from Fig. 2D and Fig. 3. Cigna et al. does not teach the interconnect array constructed of integrated circuits and used as a readout device; however, it is inherent that an interconnect array in a detector array is constructed using microelectronic integrated circuits, and that such an interconnect array is used as a readout device in a hybrid detector array. Cigna et al. does not teach the first region comprising a first semiconductor region and the second region comprising a second semiconductor region. It is common knowledge that photodetectors are constructed using semiconducting materials. It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the first and second region of the detector array of Cigna et al. with semiconductor material, to provide commonly used detector elements for each island.

Regarding Claim 5, Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect used to hybridize the islands (see Col. 4, lines 6-8). Cigna et al. does not teach the input/output element as an emitter. It would have been obvious to one of ordinary skill

in the art at the time the invention was made to construct the array of Cigna et al. with emitter elements instead of detector elements, to provide an emitter array with similar signal-isolation properties as the detector array.

Regarding Claim 9, it would have been obvious to one of ordinary skill in the art at the time the invention was made to n-dope the first semiconductor region and p-dope the second semiconductor region, as the dopant characteristics of one n-type and one p-type region allow for improved current flow, and it is design choice which region is designated as which type.

Regarding Claims 16 and 17, Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect. Cigna et al. also teach the detector islands electrically isolated from each of the other detector islands except through the readout integrated circuit array, as the readout integrated circuit array provides the only connection between any two detector islands, as seen in Fig. 2D. It would have been obvious to one of ordinary skill in the art at the time the invention was made to provide electrical isolation of the detector islands in the detector array of Cigna et al., to reduce electrical interference from adjacent detector islands.

8. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Cigna et al. in view of Izumi et al. US Patent No. 6,262,408.

Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect.

Cigna et al. do not teach an electrically nonconducting support material lying between the readout integrated circuit array and the detector array. Izumi et al. teach a detector array with conductive bump interconnects (8) (see Fig. 1) with an electrically nonconducting support material (7) lying between the top and bottom interconnects. It would have been obvious to one of ordinary skill in the art at the time the invention was made to add the nonconducting support material of Izumi et al. between the first/second regions and the readout integrated circuit array of the detector array of Cigna et al., to provide improved stability due to a greater contact surface area.

9. Claims 7, 11, 13-15, 18-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cigna et al. in view of Dodd US Patent No. 6,157,042.

Regarding Claims 14 and 15, Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect. Cigna et al. do not teach the first and second bump interconnect comprising indium, and does not teach the detector array type consisting from mercury-cadmium-telluride, indium antimonide, quantum well infrared photodetector, or extrinsic impurity band conductor material. Dodd teaches a detector array containing a bump interconnect structure (80), where the bump comprises indium (see Col 4, lines 1-2). Dodd also teaches the use of mercury cadmium telluride diode technology (see Col 1, line 9-11) and quantum well infrared photodetector (see Col. 1, lines 13-18) as photodetector material common in the art of photodetection. It is also common knowledge that indium antimonide is a semiconductor material used in a photodetector, and that extrinsic impurity band conductor materials are commonly used for infrared

photodetectors. Regarding Claim 14, it would have been obvious to one of ordinary skill in the art at the time the invention was made to comprise the bump interconnects of indium from Dodd with the detector array of Cigna et al., to provide a conductive bump connection between the detector and the interconnect array. Regarding Claim 15, it would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the detector array from one of the group of mercury-cadmium-telluride, indium antimonide, quantum well infrared photodetector, or extrinsic impurity band conductor material, as such photodetecting techniques are well known in the art, as taught by Dodd.

Regarding Claims 18 and 19, Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect. Cigna et al. do not teach the second region overlying the first region. Dodd teaches a detector array with a bump interconnect (80), a first semiconductor region (70), a second semiconductor region (66A-66D), and a readout integrated circuit element (81), where the second semiconductor region overlies the first semiconductor region. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the detector array of Cigna et al. with the semiconductor region layouts taught by Dodd, to enhance the photodetecting process and isolate the detector islands from electrical interference.

Regarding Claim 20, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form a trench through the first and second semiconductor region and into the detector substrate in the detector array of Cigna et al. in view of Dodd, as a trench

would provide the electrical isolation between adjacent detector islands by separating the first and second semiconductor regions between adjacent detector islands as seen in Fig. 3D of Dodd.

Regarding Claim 21, it would have been obvious to one of ordinary skill in the art at the time the invention was made to remove the detector substrate, to provide a maximal electrical connection through the bump interconnects between the semiconductor regions and the readout integrated circuit.

Regarding Claims 7, 13, and 22, Cigna et al. teach a detector array with island elements each containing a first and second region, an interconnect array with each element containing a first and second detector interconnection, and a bump interconnect structure with a first and second bump interconnect. Cigna et al. do not teach the detector array or the readout integrated circuit array having a curved shape. Dodd teaches the detector elements being able to contain a curved configuration (see Col. 9, lines 34-36). It is also common knowledge an integrated circuit array can possess a curved shape to correspond to a curved detector. It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the detector array and readout integrated circuit array of Cigna et al. with the curved configuration taught by Dodd, to provide an improved scanning accuracy.

Regarding Claims 11 and 23, it would have been obvious to one of ordinary skill in the art at the time the invention was made to comprise the readout integrated circuit array with an electrical conductor interconnecting all the first detector interconnect locations, to provide a common signal among all the detector islands through the readout integrated circuit array.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stephen Yam whose telephone number is (703)306-3441. The examiner can normally be reached on Monday-Friday 8:30am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Frank Font can be reached on (703)308-4881. The fax phone numbers for the organization where this application or proceeding is assigned are (703)308-7724 for regular communications and (703)308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

SY S.Y
May 29, 2002

Kevin Pyo
Primary Examiner